

## N-Channel Enhancement Mode Power MOSFET

### Description

The PT100S uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

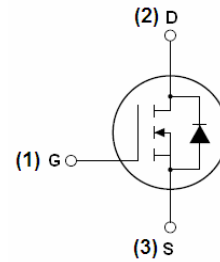
- $V_{DS} = 70V, I_D = 1A$   
 $R_{DS(ON)} < 10.5m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low  $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- PWM
- Load Switching

100% UIS TESTED!

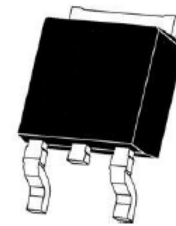
100%  $\Delta V_{DS}$  TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
PT100S	PT100S	TO-252-2L	7" REEL	12mm	3000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	70	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	1A	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	0.5A	A
Pulsed Drain Current	$I_{DM}$	3A	A
Maximum Power Dissipation	$P_D$	110	W
Derating factor		0.73	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	$E_{AS}$	320	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.36	°C/W
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

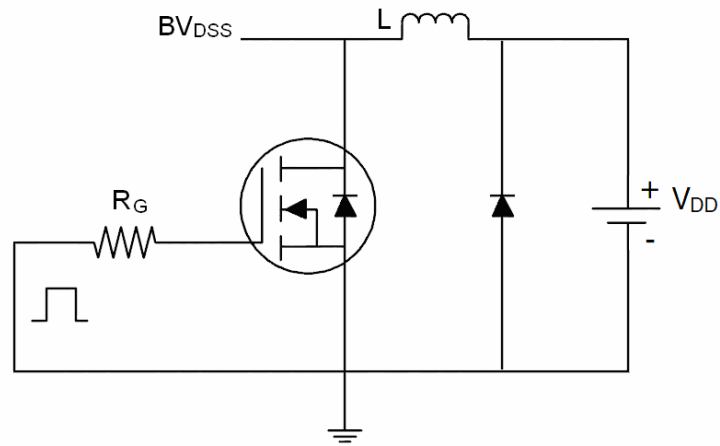
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	70	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =70V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	2	2.8	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	9.3	10.5	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V,I <sub>D</sub> =20A	20	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =35V,V <sub>GS</sub> =0V, F=1.0MHz	-	3418.9	-	PF
Output Capacitance	C <sub>oss</sub>		-	199	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	135	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =35V,R <sub>L</sub> =1Ω V <sub>GS</sub> =10V,R <sub>G</sub> =3Ω	-	8.5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	7	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =35V,I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	65		nC
Gate-Source Charge	Q <sub>gs</sub>		-	16.5		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	15.3		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =20A	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	80	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF = 20A di/dt = 100A/μs <sup>(Note3)</sup>	-	32	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	45	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

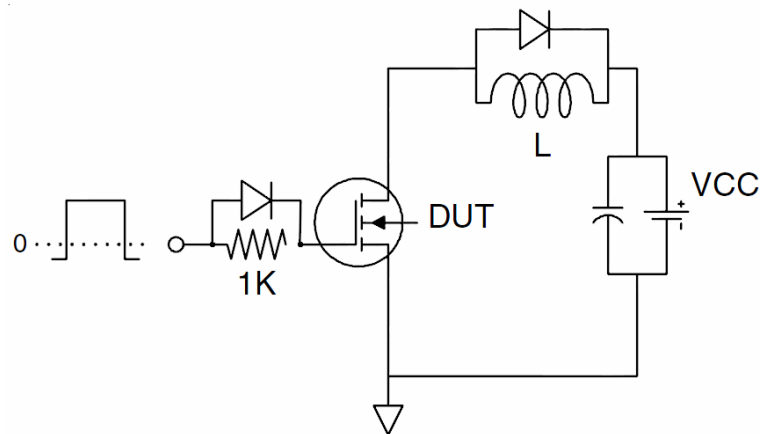
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition :  $T_J=25^{\circ}\text{C}, V_{DD}=35V, V_G=10V, L=0.5mH, R_G=25\Omega$

## Test circuit

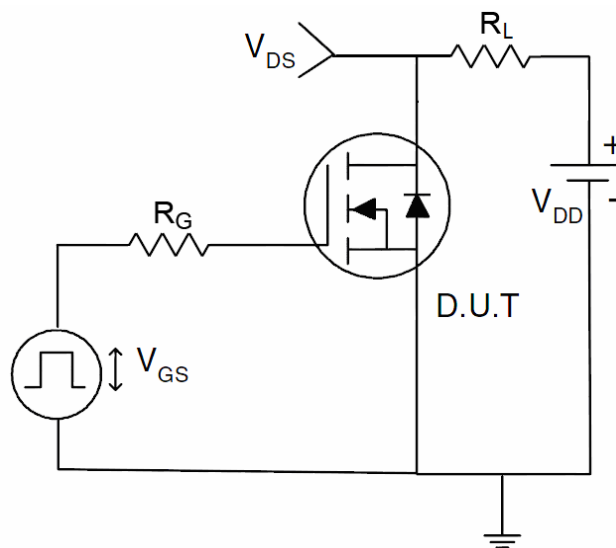
### 1) $E_{AS}$ Test Circuit



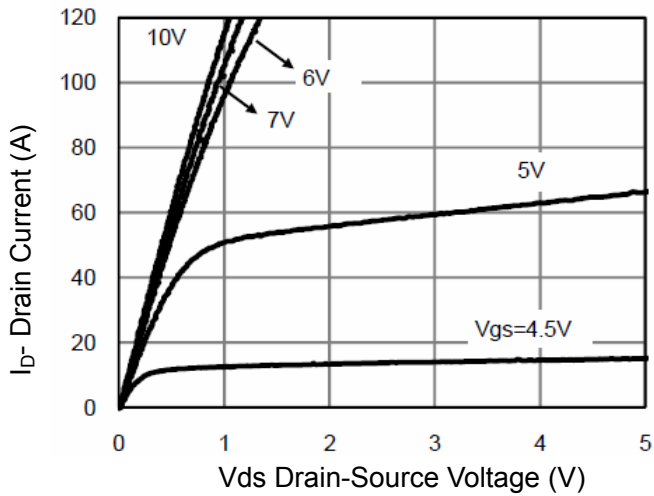
### 2) Gate Charge Test Circuit



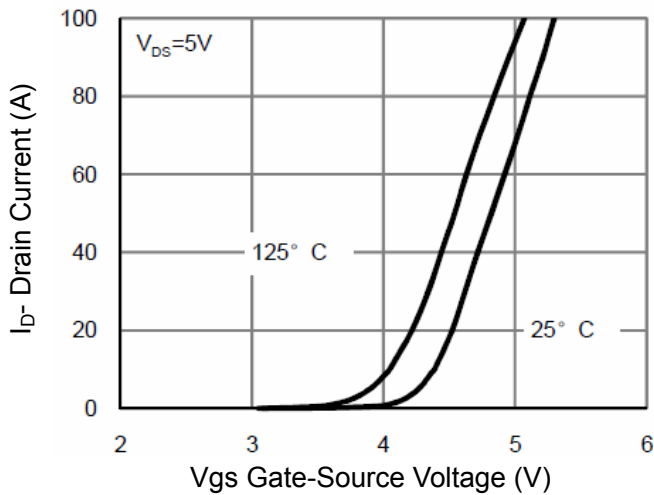
### 3) Switch Time Test Circuit



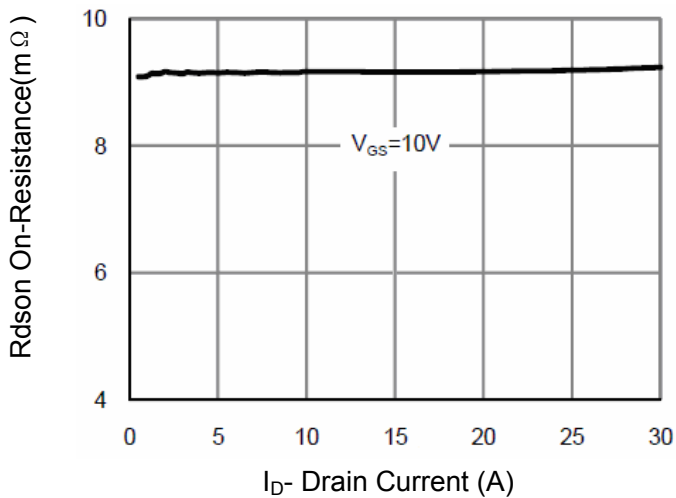
## Typical Electrical and Thermal Characteristics (Curves)



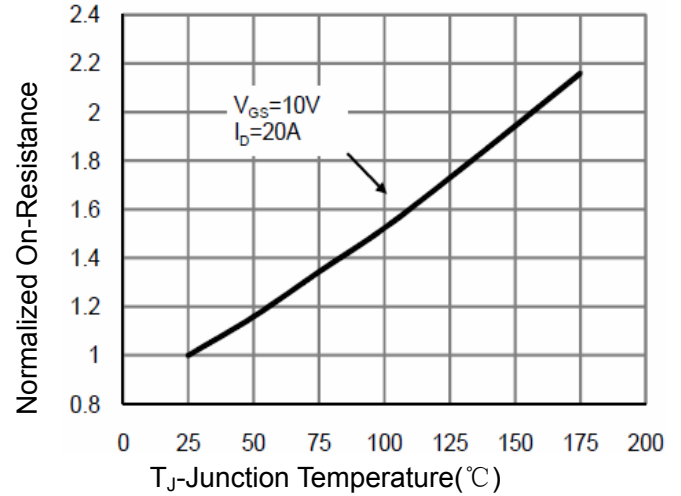
**Figure 1 Output Characteristics**



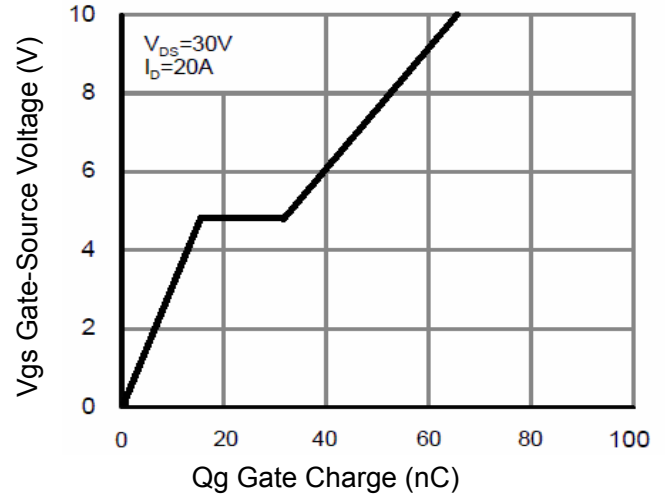
**Figure 2 Transfer Characteristics**



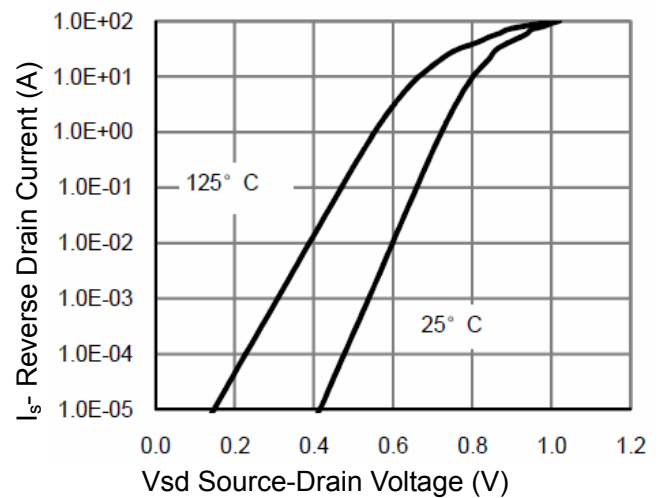
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

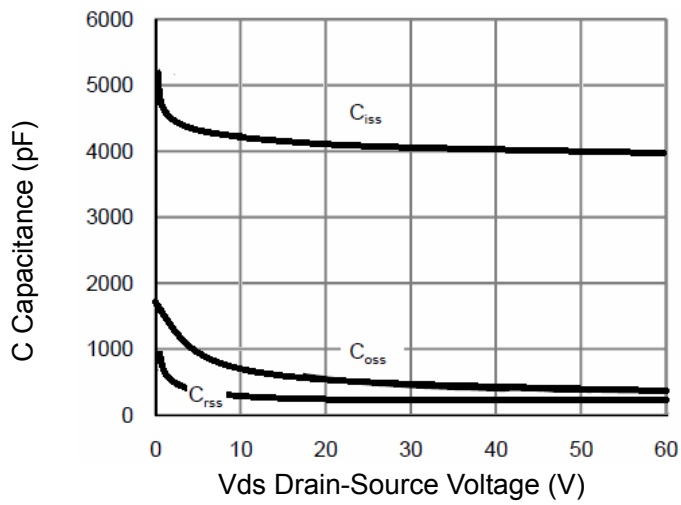


Figure 7 Capacitance vs Vds

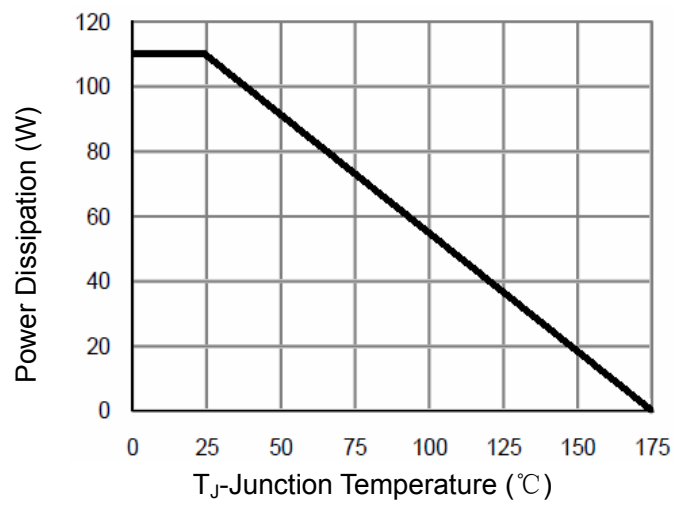


Figure 9 Power De-rating

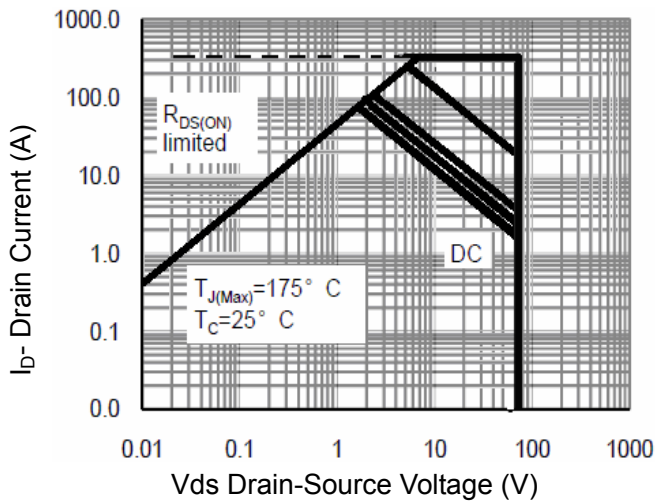


Figure 8 Safe Operation Area

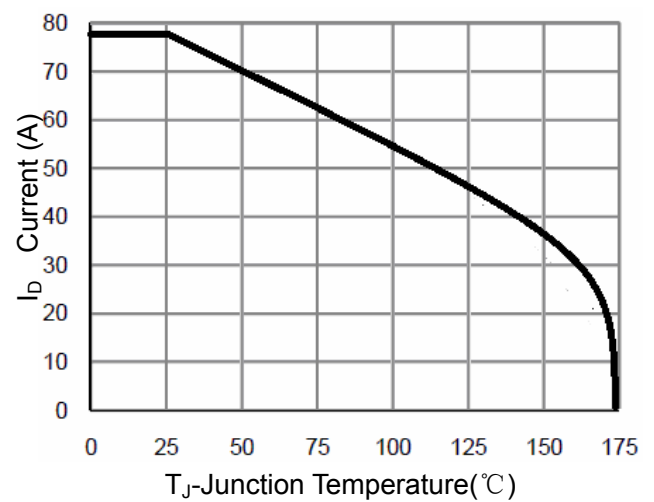


Figure 10  $I_D$  Current- Junction Temperature

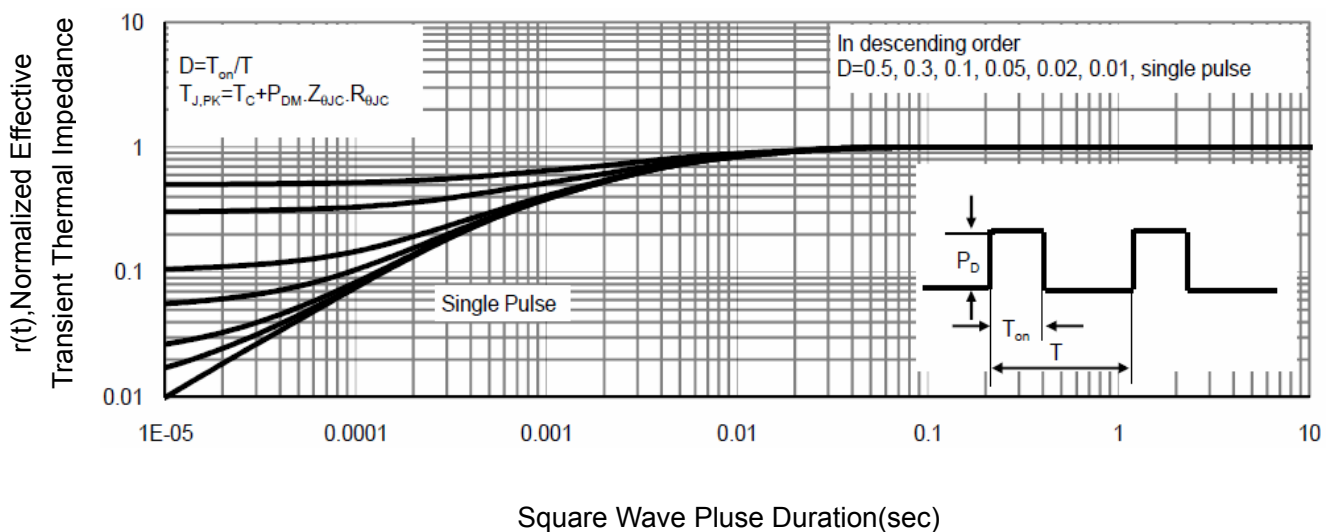
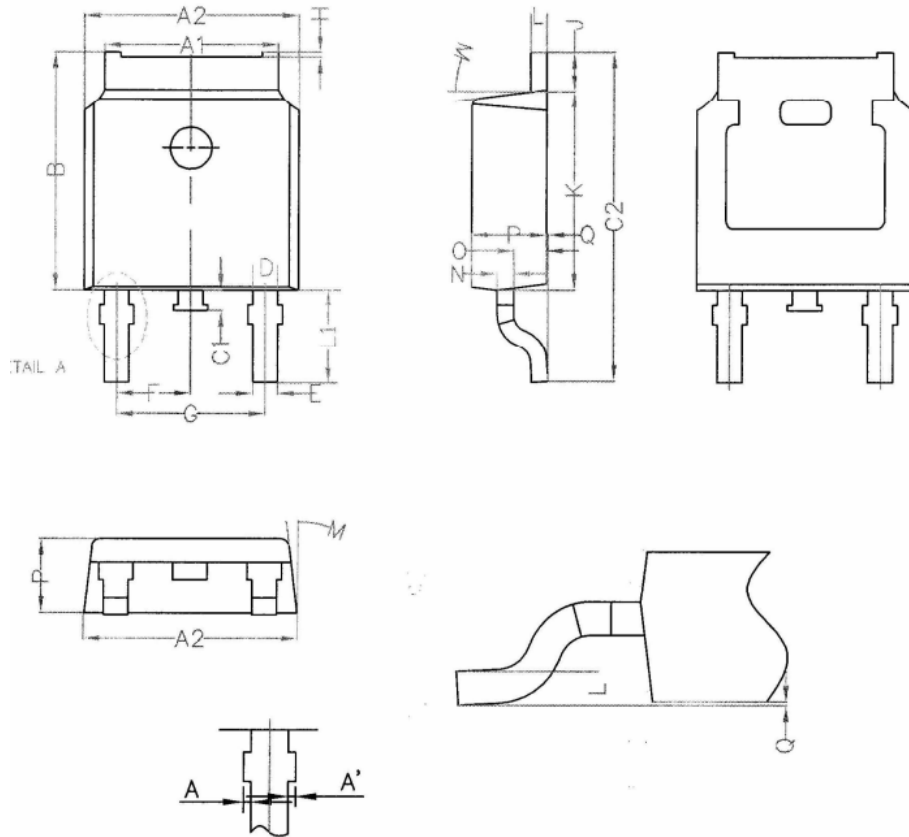


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D		1.00	
E		0.76	
F		2.286	
G		4.572	
H		0.15	
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L		0.508	
L1	2.65	2.80	2.95
M		7°	
N		0.508	
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q		0.05	0.10