

### GENERAL DESCRIPTION

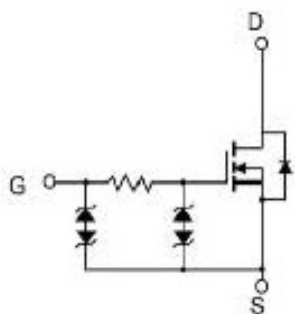
The HM3400KR is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

### FEATURES

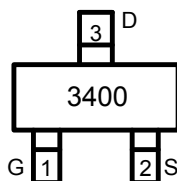
- $R_{DS(ON)} = 450 \text{ m}\Omega$  @  $V_{GS} = 4.5\text{V}$
- $R_{DS(ON)} = 550 \text{ m}\Omega$  @  $V_{GS} = 2.5\text{V}$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch



N-Channel



Marking and pin Assignment



SOT-323 top view

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V

### Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±10	V

### Electrical Characteristics (T<sub>j</sub>=25°C Unless Otherwise Specified)

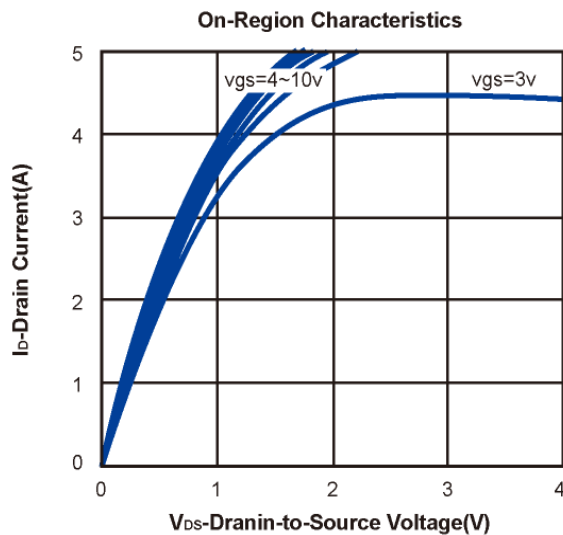
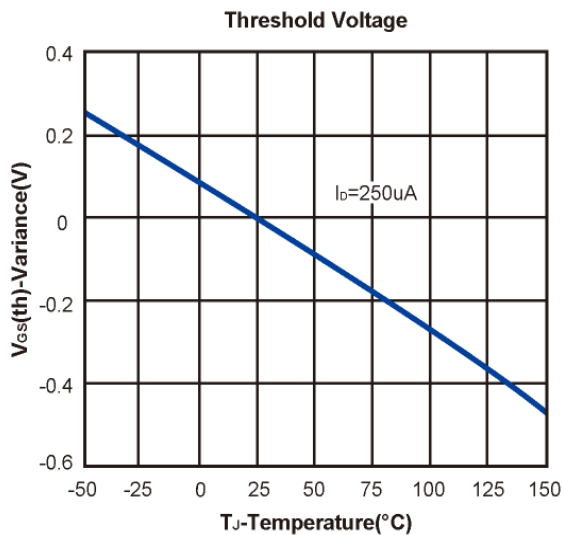
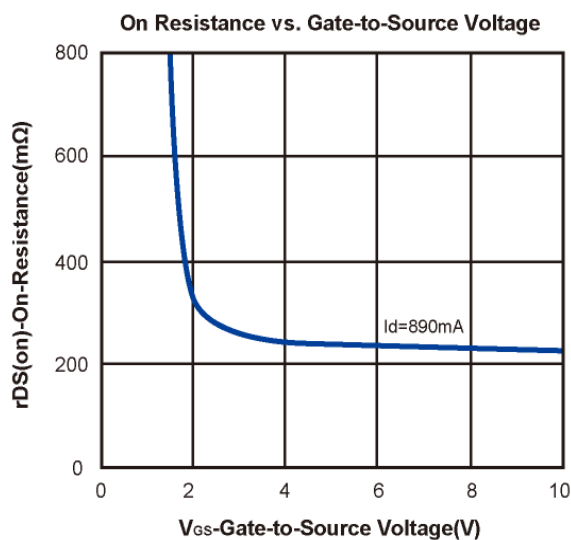
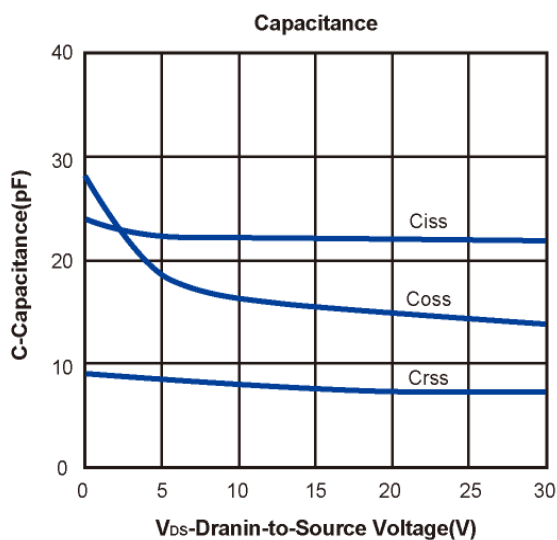
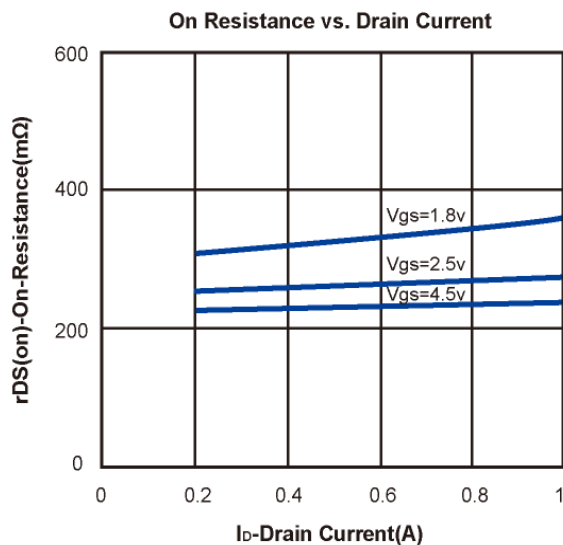
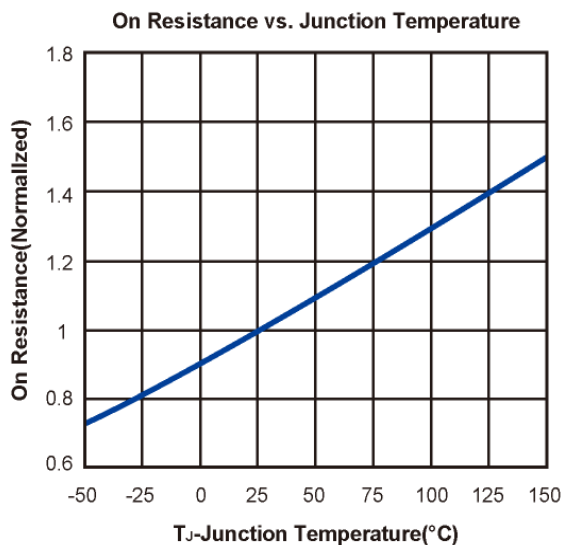
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	0.5	1.0	1.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			±10	μA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(on)</sub>	Drain-Source On-Resistance <sup>a</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =800mA		280	450	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =780mA		370	550	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =350mA, V <sub>GS</sub> =0V		0.75	1.2	V
<b>DYNAMIC</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ		21		pF
C <sub>OSS</sub>	Output Capacitance			15		
C <sub>rss</sub>	Reverse Transfer Capacitance			8		
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =25V, V <sub>GS</sub> =10V, I <sub>D</sub> =0.22A		6.7		nC
Q <sub>gs</sub>	Gate-Source Charge			1.2		
Q <sub>gd</sub>	Gate-Drain Charge			0.9		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =10V, R <sub>L</sub> =3Ω V <sub>GEN</sub> =10V, R <sub>G</sub> =10Ω		120		ns
t <sub>r</sub>	Turn-On Rise Time			317		
t <sub>d(off)</sub>	Turn-Off Delay Time			748		
t <sub>f</sub>	Turn-Off Fall Time			716		

Notes: a. Based on epoxy or solder paste and bond wire Cu wire 1mil×1(S), Cu wire 1mil×1(G) on each die of SOT-523 package.

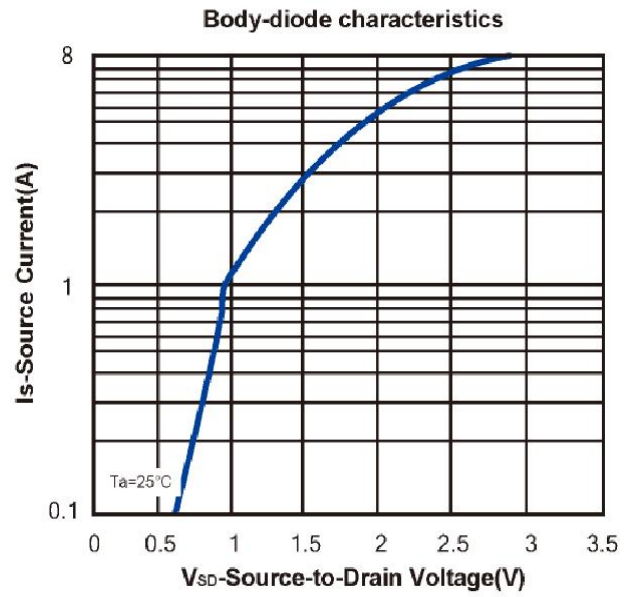
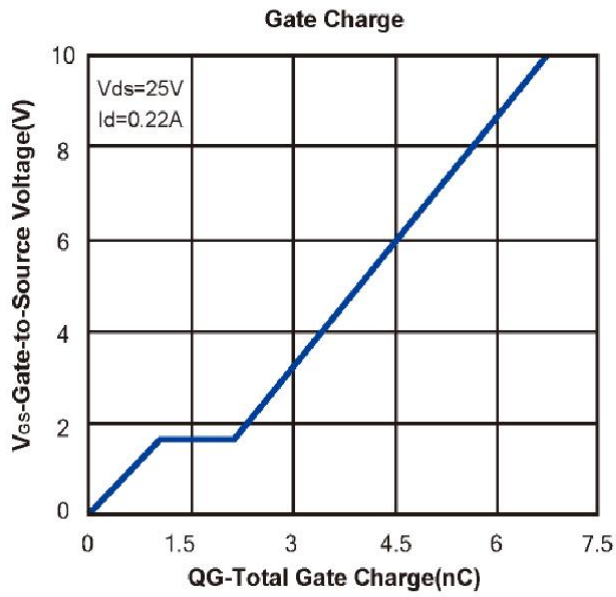
b. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%.

c. Force mos reserves the right to improve product design, functions and reliability without notice.

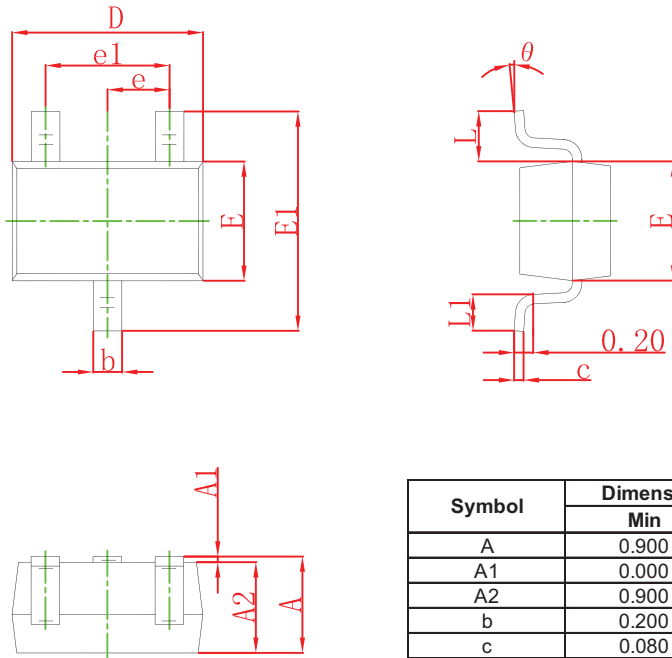
### Typical Characteristics (T<sub>J</sub> =25°C Noted)



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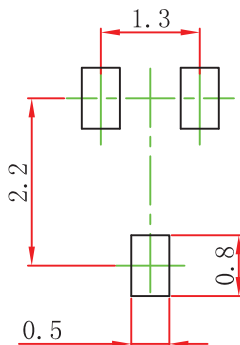


### SOT-323 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

### SOT-323 Suggested Pad Layout



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.