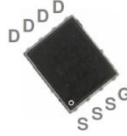
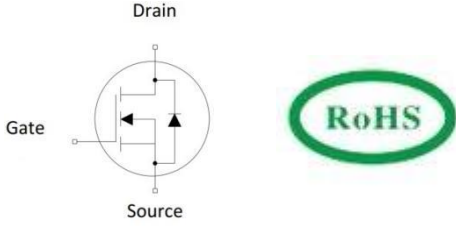


N-channel 100V, 70A, 7mΩ SGT MOSFET

<p>Description</p> <p>This power MOSFET is designed with split gate trench technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.</p> <p>Features</p> <ul style="list-style-type: none"> ◆ Very low FOM $R_{DS(on)} \times Q_g$ ◆ 100% UIS tested ◆ RoHS compliant <p>Applications</p> <ul style="list-style-type: none"> ◆ Motor Drivers. ◆ DC-DC Converter. ◆ Uninterrupted power supply (UPS). 	<p>Product Summary</p> <table> <tr> <td>$V_{DS} @ T_{j,25^\circ C}$</td><td>100V</td></tr> <tr> <td>$R_{DS(on),max}$</td><td>7mΩ</td></tr> <tr> <td>I_D</td><td>70A</td></tr> </table> <div style="text-align: center;">  <p>DFN5*6</p> </div> <div style="text-align: center;">  <p>N-Channel MOSFET</p> </div>	$V_{DS} @ T_{j,25^\circ C}$	100V	$R_{DS(on),max}$	7mΩ	I_D	70A
$V_{DS} @ T_{j,25^\circ C}$	100V						
$R_{DS(on),max}$	7mΩ						
I_D	70A						

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	V
Continuous drain current ($T_C = 25^\circ C$)	I_D	70	A
($T_C = 100^\circ C$)		44	A
Pulsed drain current ¹⁾	I_{DM}	280	A
Gate-Source voltage	V_{GSS}	± 20	V
Avalanche energy, single pulse ²⁾	E_{AS}	200	mJ
Power Dissipation DFN5*6 ($T_C = 25^\circ C$)	P_D	102	W
- Derate above $25^\circ C$		0.82	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	70	A
Diode pulse current	$I_{S,pulse}$	280	A

Thermal Characteristics DFN5*6

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.73	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	49	$^{\circ}\text{C/W}$
Soldering temperature, wave soldering only allowed at leads. (1.6mm from case for 10s)	T_{sold}	260	$^{\circ}\text{C}$

Electrical Characteristics $T_c = 25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250uA	100	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1		3	V
Drain cut-off current	I _{DSS}	V _{DS} =100 V, V _{GS} =0 V, T _j = 25°C T _j = 125°C	- -	- 10	1 -	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =20 V, V _{DS} =0 V	-	-	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-20 V, V _{DS} =0 V	-	-	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =35 A T _j = 25°C	- - -	7	8.6 -	mΩ
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1MHz	-	3041	-	pF
Output capacitance	C _{oss}		-	486	-	
Reverse transfer capacitance	C _{rss}		-	12	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 50V, I _D = 35A R _G = 25Ω, V _{GS} =10V	-	16	-	ns
Rise time	t _r		-	50	-	
Turn-off delay time	t _{d(off)}		-	135	-	
Fall time	t _f		-	90	-	
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DD} =80 V, I _D =35A, V _{GS} =0 to 10 V	-	8.6	-	nC
Gate to drain charge	Q _{gd}		-	9.1	-	
Gate charge total	Q _g		-	42	-	
Gate plateau voltage	V _{plateau}		-	2.5	-	V
Reverse diode characteristics						
Diode forward voltage	V _{SD}	V _{GS} =0 V, I _F =35A	-	0.85	-	V
Reverse recovery time	t _{rr}	V _R =50 V, I _F =35A,	-	72	-	ns
Reverse recovery charge	Q _{rr}	dI _F /dt=100 A/μs	-	110	-	nC

Notes:

- Limited by maximum junction temperature, maximum duty cycle is 0.75.
- $I_{AS} = 20\text{ A}, V_{DD} = 50\text{ V},$ Starting $T_j = 25^{\circ}\text{C}.$
- Repetitive Rating: Pulse width limited by maximum junction temperature.

Electrical Characteristics Diagrams

Figure 1. Output Characteristics

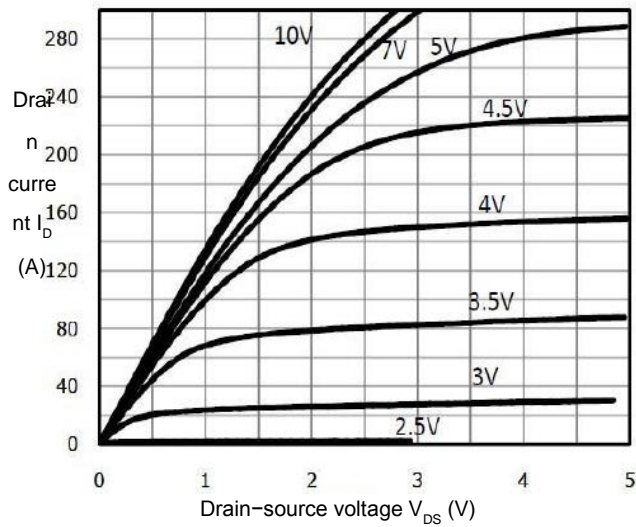


Figure 2. Transfer Characteristics

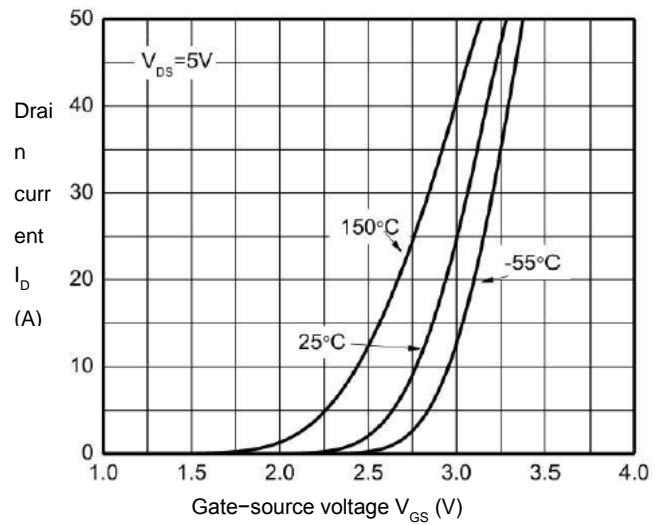


Figure 3. On-Resistance vs. Drain Current

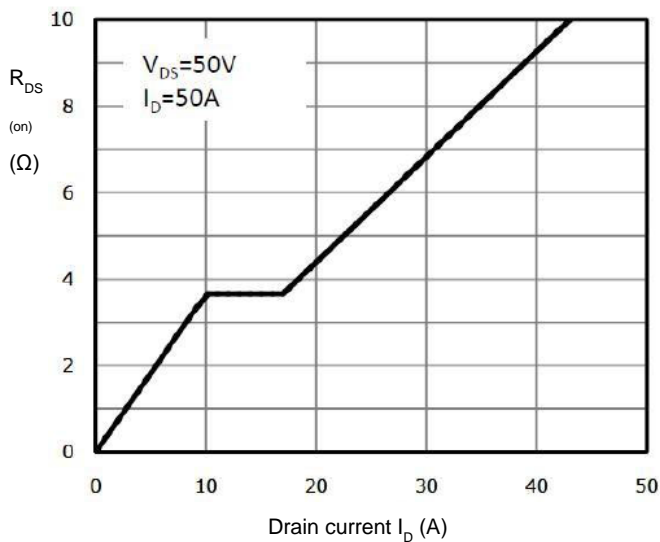


Figure 4. Capacitance Characteristics

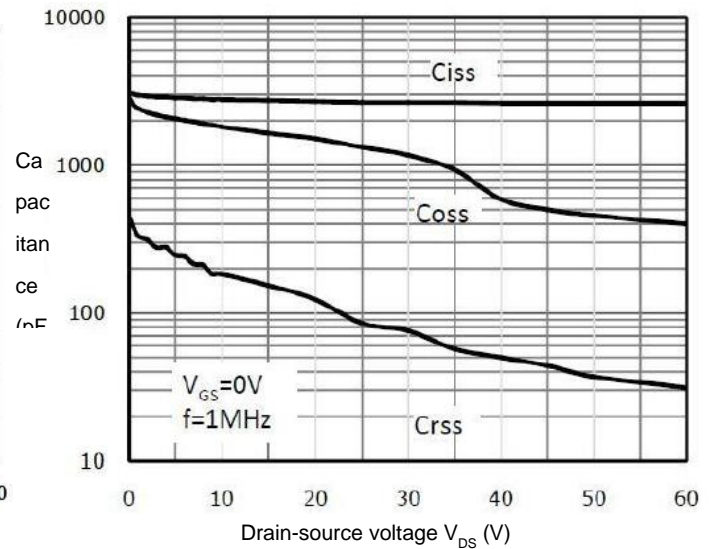


Figure 5. Gate Charge Characteristics

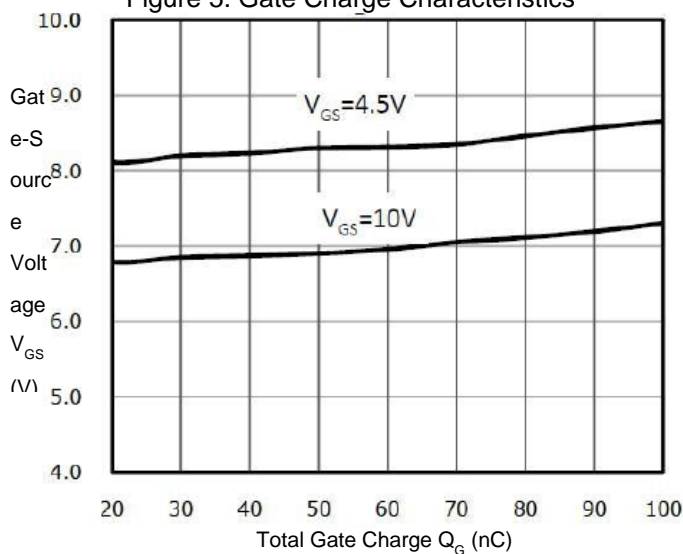


Figure 6. Body Diode Forward Voltage

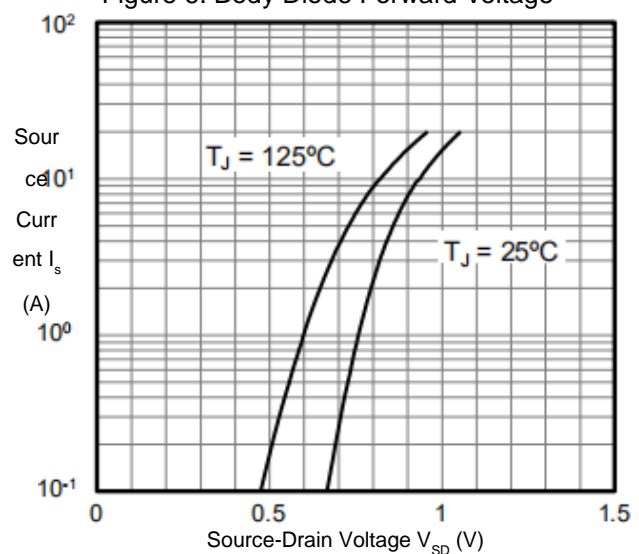


Figure 7. Breakdown Voltage vs. Temperature

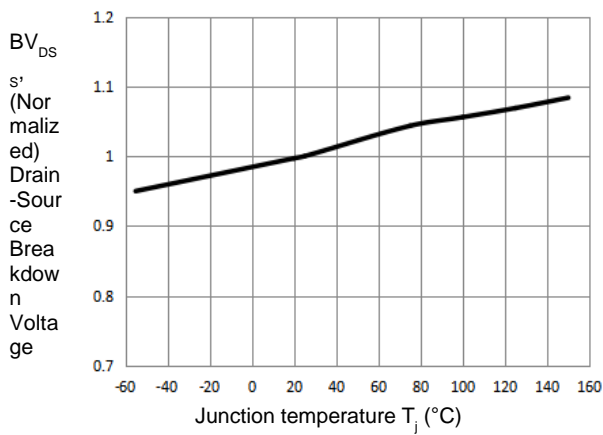


Figure 8. On-Resistance vs. Temperature

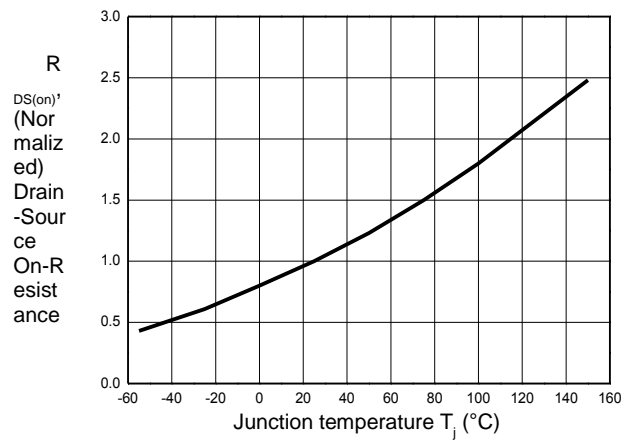


Figure 9. Transient Thermal Impedance

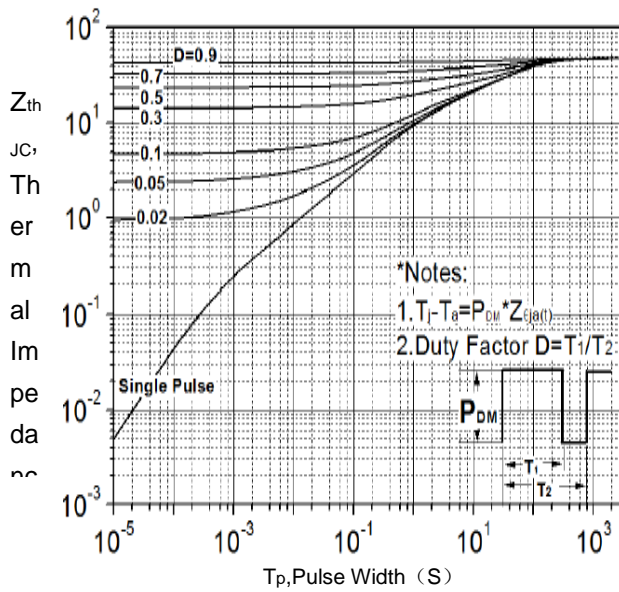
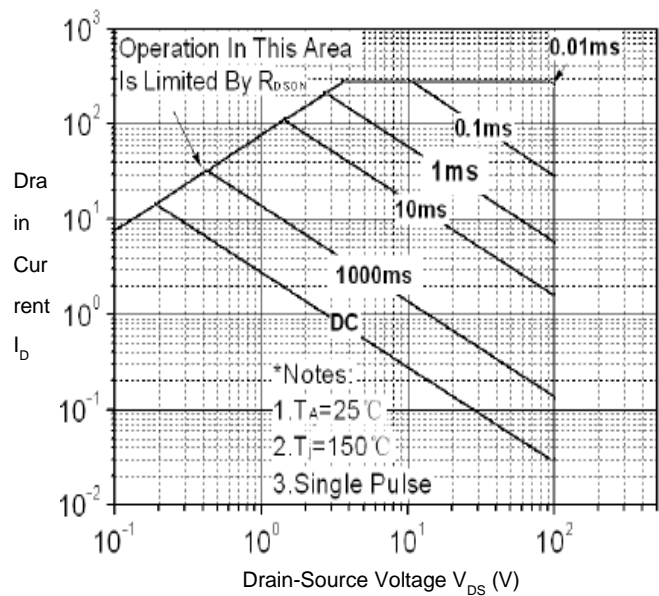
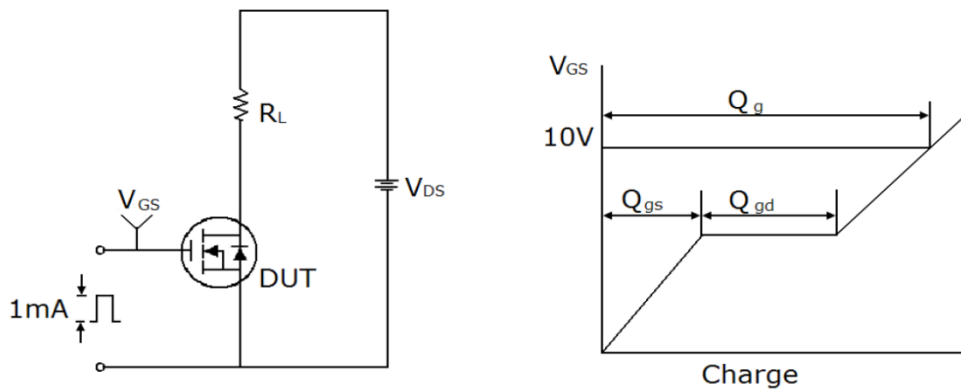


Figure 10. Maximum Safe Operating Area

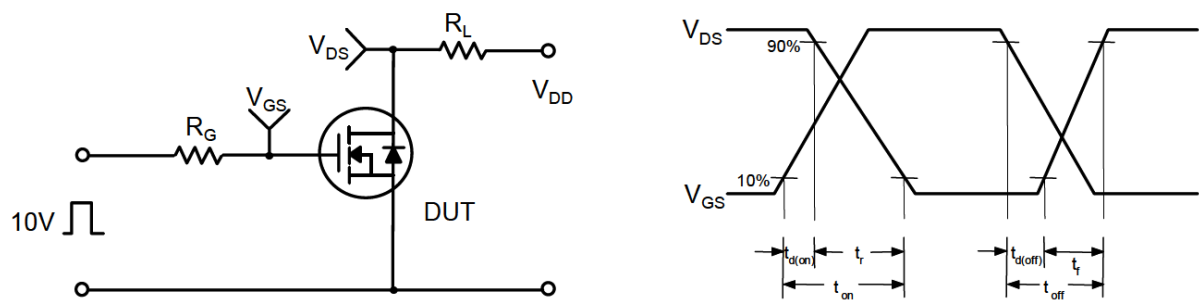


Test Circuits

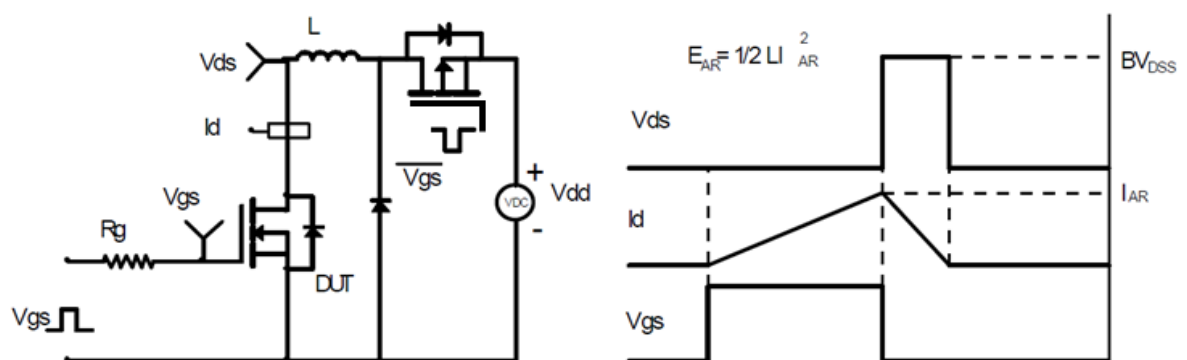
Gate Charge Test Circuit & Waveform



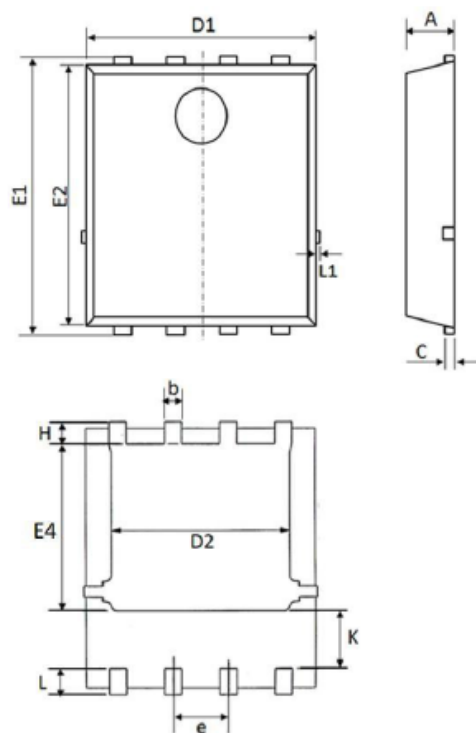
Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



Mechanical Dimensions for DFN5*6



COMMON DIMENSIONS						
SYMBOL	MILLIMETERS			INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1	1.1	1.2	0.039	0.043	0.047
b	0.3	0.4	0.5	0.012	0.016	0.020
C	0.154	0.254	0.354	0.006	0.010	0.014
D1	5	5.2	5.4	0.197	0.205	0.213
D2	3.8	4.1	4.25	0.150	0.161	0.167
E1	5.95	6.15	6.35	0.234	0.242	0.250
E2	5.66	5.86	6.06	0.223	0.231	0.239
E4	3.52	3.72	3.92	0.139	0.146	0.154
e	1.27 BSC			0.050 BSC		
H	0.4	0.5	0.6	0.016	0.020	0.024
L	0.5	0.6	0.7	0.020	0.024	0.028
L1	-	-	0.12	-	-	0.005
K	1.14	1.29	1.44	0.045	0.051	0.057