HM2380DR

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-20V	±12V	18mR@-4V5	-7.5A
		21mR@-2V5	
		28mR@-1V8	
		40mR@-1V5	

➢ Description

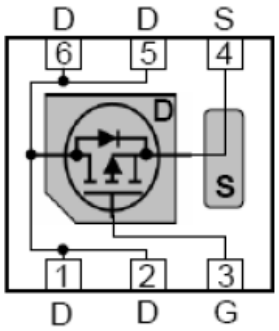
This device is produced with high cell density DMOS trench technology, uses advanced trench technology and design to provide excellent RDSON with low gate charge. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

➢ Applications

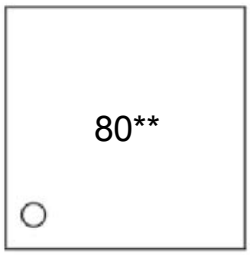
- Load Switch
- Portable Devices
- DCDC conversion
- Charging
- Driver for Relay

➢ Pin configuration

Top view



Bottom View



Marking

➢ Ordering Information

Device	Package	Shipping
HM2380DR	DFN2x2	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	-7.5	A
I_{DM}	Pulsed Drain Current [b]	-24	A
P_D	Power Dissipation [c]	3	W
P_{DSM}	Power Dissipation [a]	1.4	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		99	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		45	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

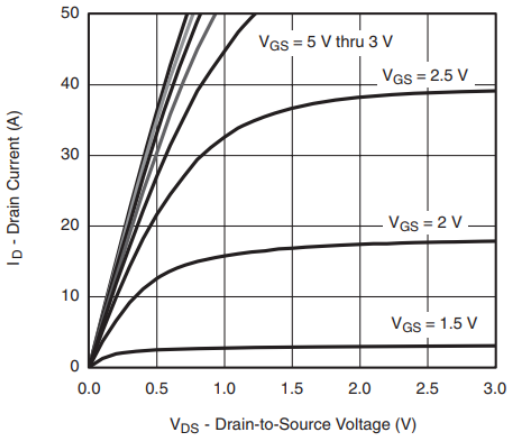
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

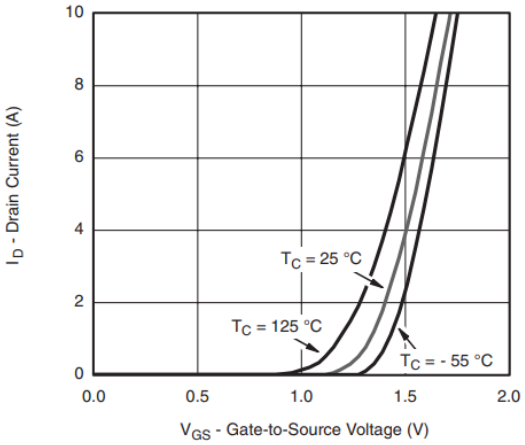
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V , ID=-250uA	-20			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS , ID=-250uA	-0.45	-0.55	-0.8	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-4.5V , ID=-5.5A		18	26	mR
		VGS=-2.5V , ID=-2.5A		21	30	
		VGS=-1.8V , ID=-1.8A		28	40	
		VGS=-1.5V , ID=-1.5A		40	70	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-20V , VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V , VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V , ID=-5.5A		23		S
V_{SD}	Forward Voltage	VGS=0V , IS=-1A		-0.75	-1.5	V
Ciss	Input Capacitance	VDS=-10V , VGS=0V, f=1MHz		1970		pF
Coss	Output Capacitance			205		
Crss	Reverse Transfer Capacitance			195		
$T_{D(ON)}$	Turn-on delay time	VGS=-4.5V, VDS=-10V, RL=6R, RG=6R,ID=-6.5A		16		ns
Tr	Rise time			14		
$T_{D(OFF)}$	Turn-off delay time			78		
Tf	Fall time			66		

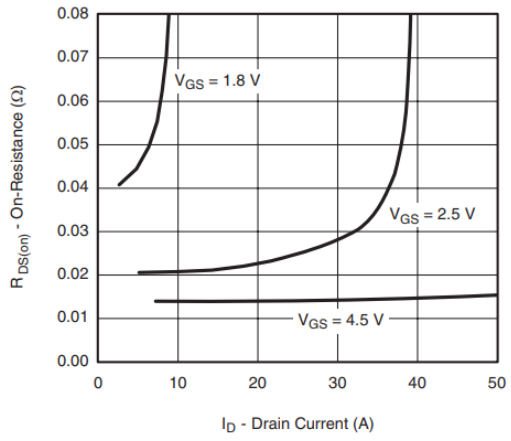
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



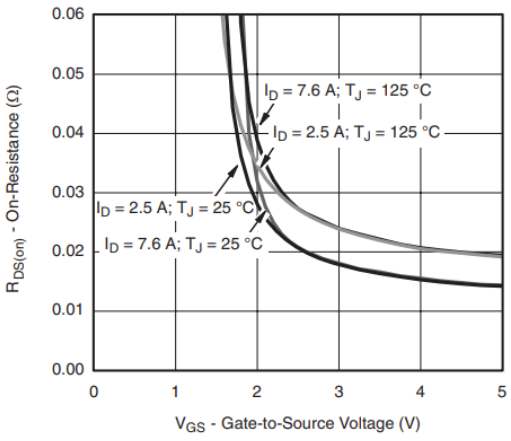
Output Characteristics



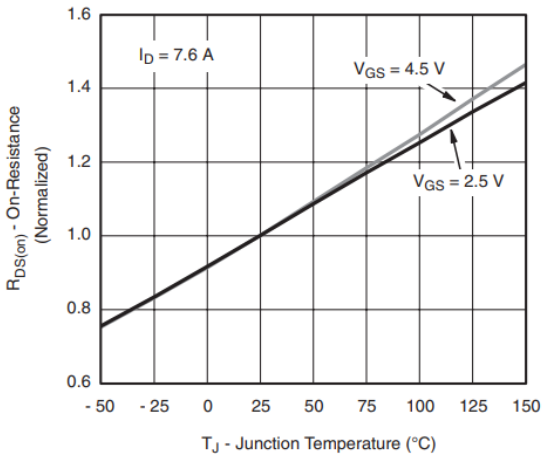
Transfer Characteristics



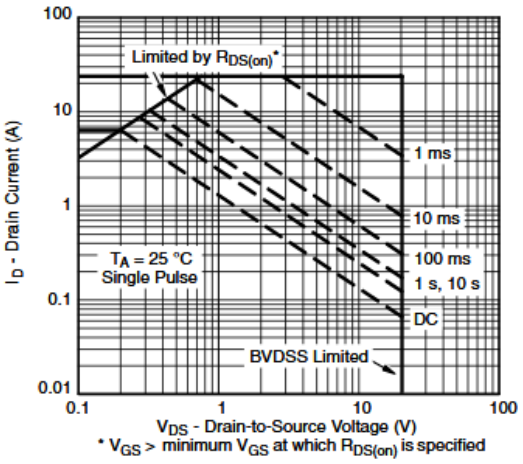
On-Resistance vs. Drain Current



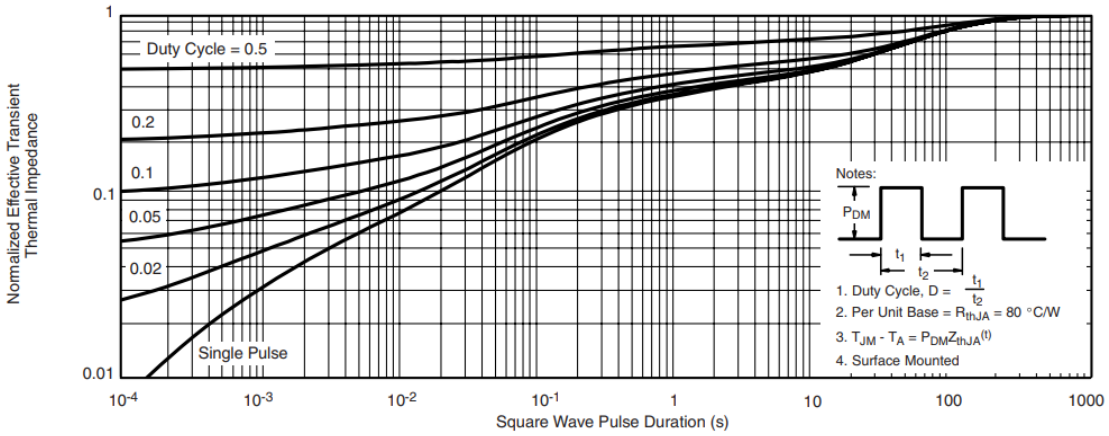
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

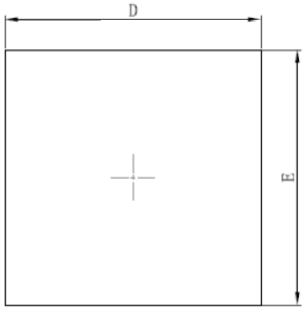


Safe Operating Area, Junction-to-Ambient

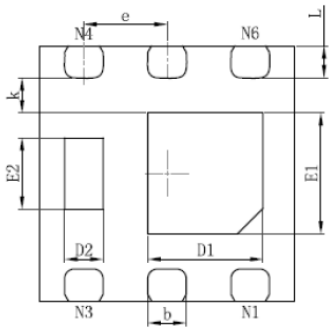


Normalized Thermal Transient Impedance, Junction-to-Ambient

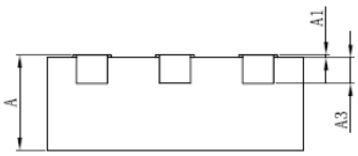
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DFN2x2-6L

Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF.	
D	1.924	2.076
E	1.924	2.076
D1	0.800	1.000
E1	0.850	1.050
D2	0.200	0.400
E2	0.460	0.660
k	0.200MIN.	
b	0.250	0.350
e	0.650TYP.	
L	0.174	0.326