HM8840Q

Dual N-Channel Enhancement-Mode MOSFET

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

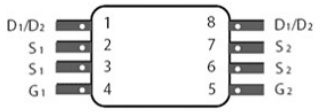
Features

For a single MOSFET

- V_{DS} = 20V
- $R_{DS(ON)}$ = 8.5mΩ @ V_{GS}=4.5V

Pin configurations

See Diagram below



(TOP VIEW) TSSOP-8

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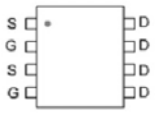

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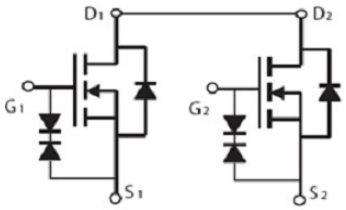


Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current	Continuous	I_D	10	A
	Pulsed		85	
Total Power Dissipation	@TA=25℃	P_D	1.7	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	20			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 16V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=10V			10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	0.3	0.65	1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=10A		8.5	9.5	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz	1000	1255	1510	pF
C_{oss}	Output Capacitance		150	220	290	pF
C_{rss}	Reverse Transfer Capacitance		100	168	235	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=10A	10	12.5	15	nC
Q_{gs}	Gate Source Charge			5.5		nC
Q_{gd}	Gate Drain Charge			6.5		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GEN}=4.5V, V_{DD}=10V, R_{GEN}=3Ω		1.1		ns
$t_{d(off)}$	Turn-Off Delay Time			7		ns
$t_{d(r)}$	Turn-On Rise Time			2.6		ns
$t_{d(f)}$	Turn-Off Fall Time			7.4		ns

Thermal Resistance

Symbol	**Parameter**	**Typ**	**Max**	**Units**
$R_{\theta JC}$	Thermal Resistance Junction to Case(t≤10s)	30	40	℃/W

Typical Characteristics

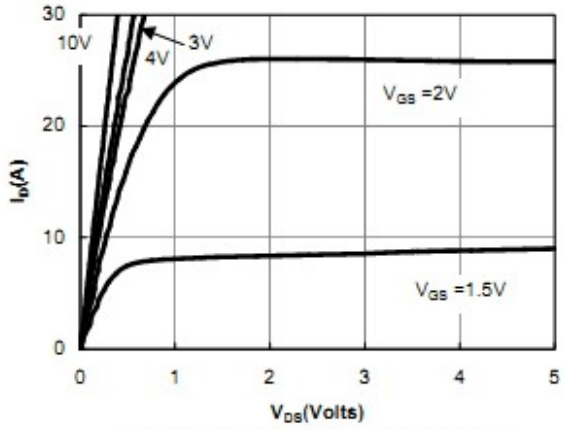


Figure 1: On-Regions CharacteristiCS

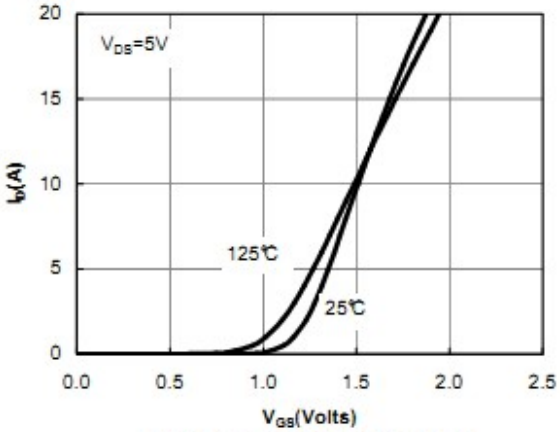


Figure 2: Transfer Characteristics

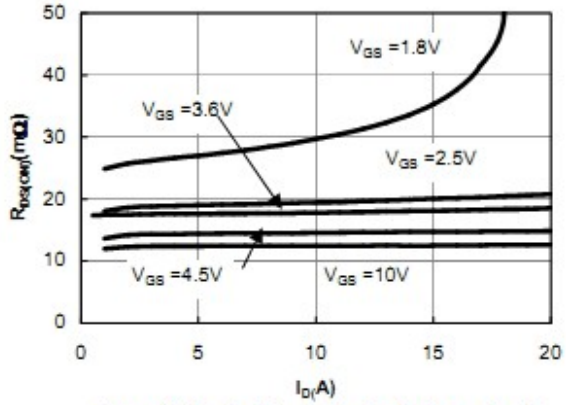


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

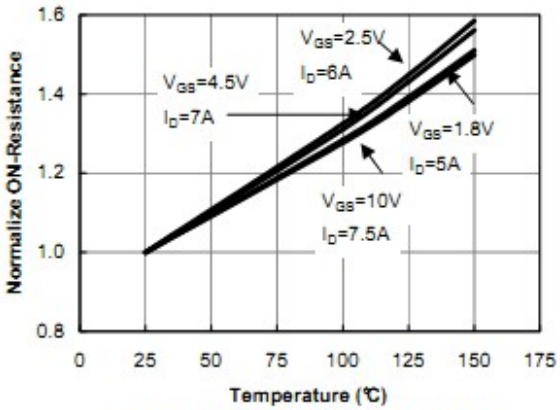


Figure 4: On-Resistance vs. Junction Temperature

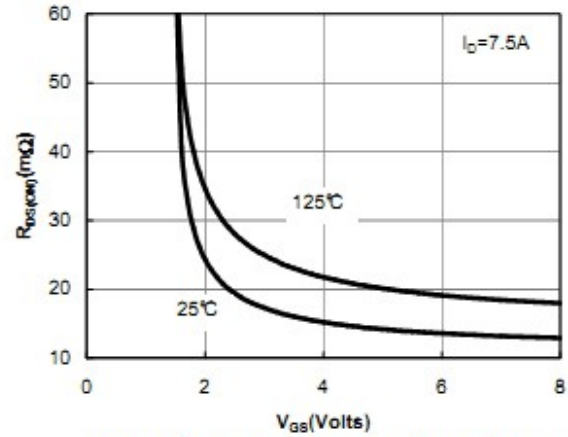


Figure 5: On-Resistance vs. Gate-Source Voltage

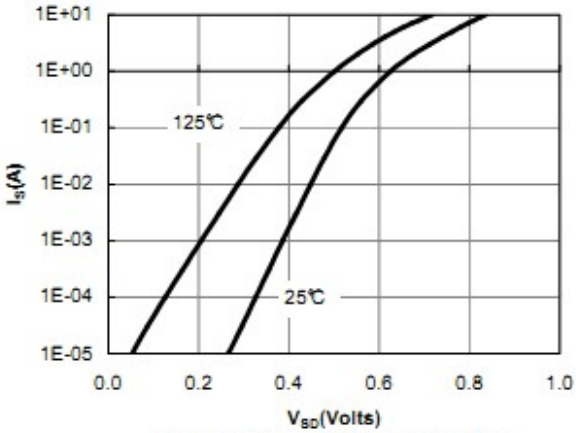


Figure 6: Body-Diode Characteristics

Typical Characteristics

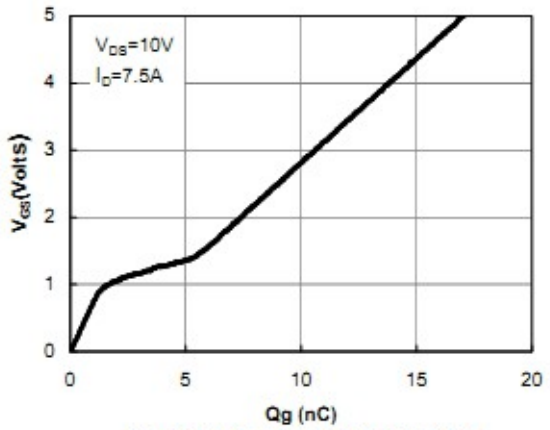


Figure 7: Gate-Charge Characteristics

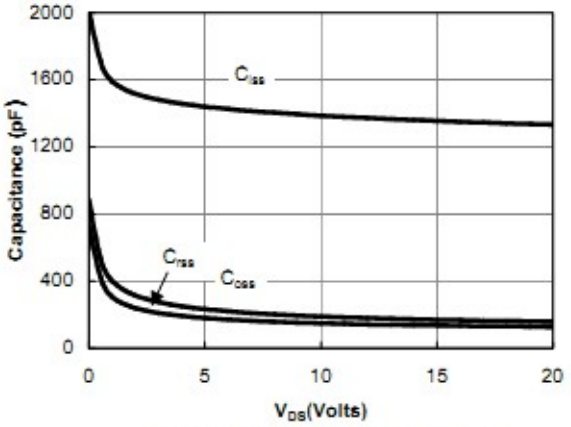


Figure 8: Capacitance Characteristics

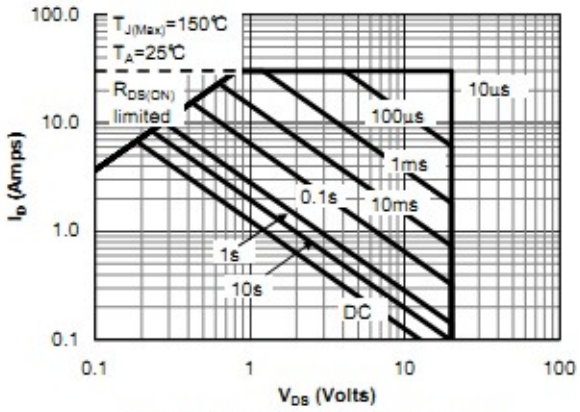


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

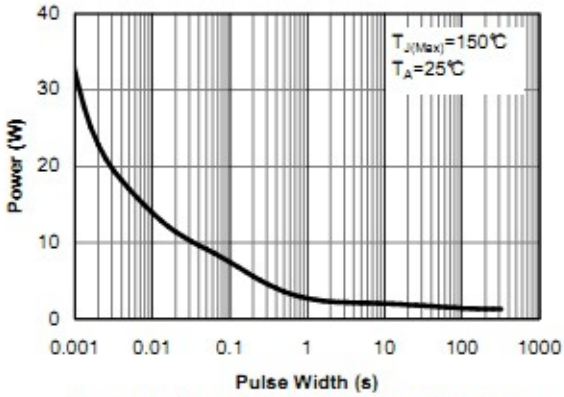


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

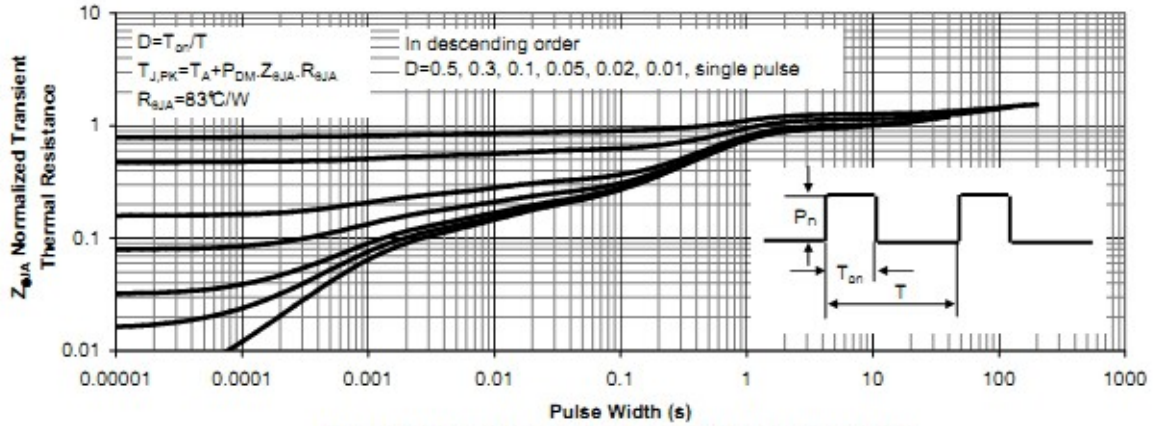
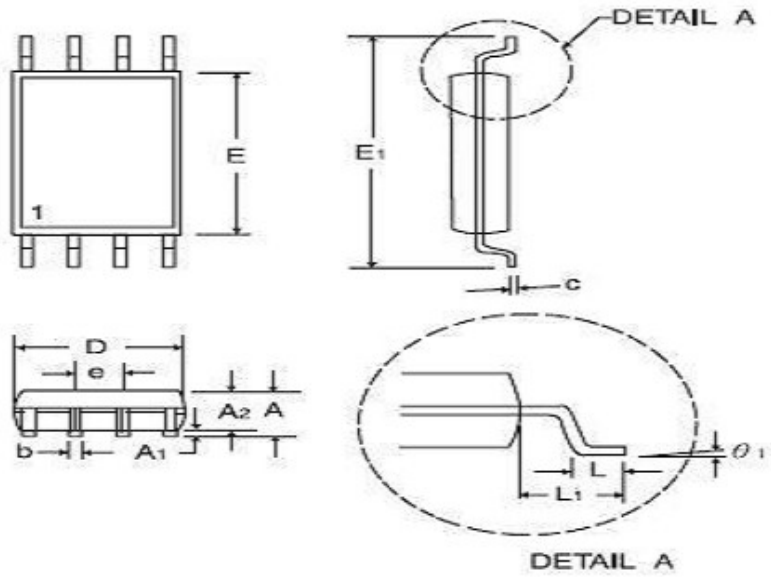


Figure 11: Normalized Maximum Transient Thermal Impedance

Package Outline Dimension

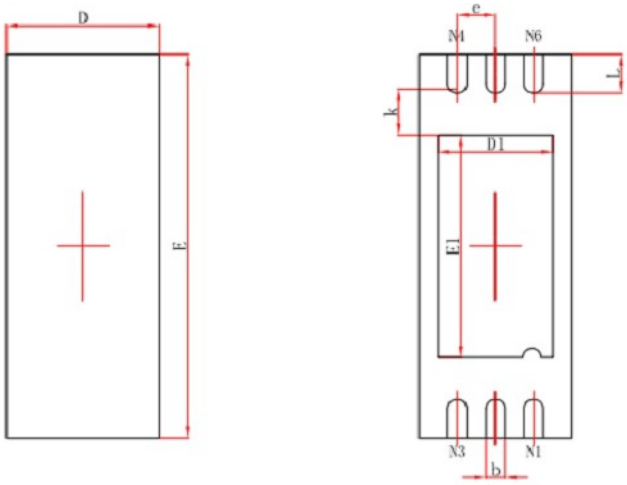
TSSOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.05	1.20	0.041	0.047
A1	0.05	0.15	0.002	0.006
A2	-	1.05	-	0.041
b	0.20	0.28	0.008	0.011
c	0.127		0.005	
D-8	2.90	3.10	0.114	0.122
E	4.30	4.50	0.169	0.177
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
θ_1	0°	8°	0°	8°

Package Outline Dimension

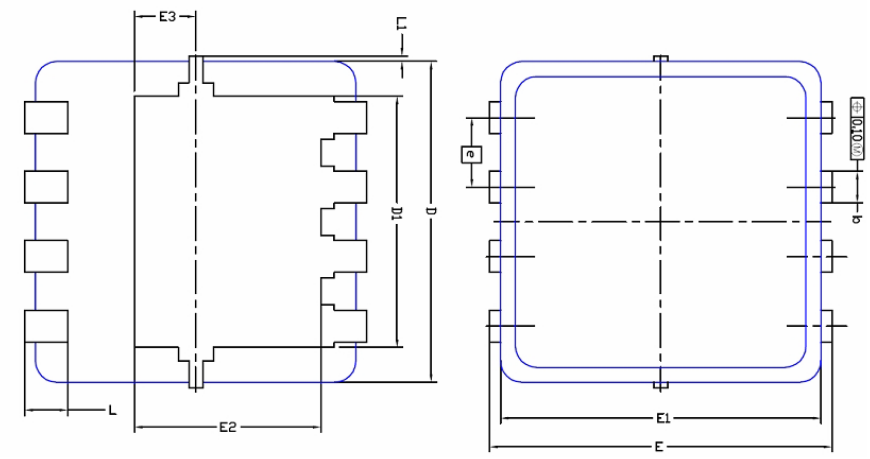
DFN5X2

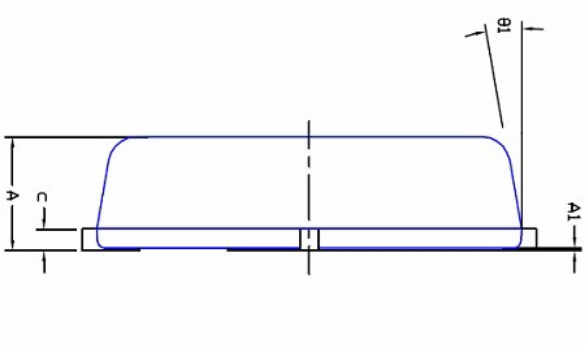


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	4.924	5.076	0.194	0.200
D1	1.400	1.600	0.055	0.063
E1	2.800	3.000	0.110	0.118
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.374	0.526	0.015	0.021

Package Outline Dimension

DFN3X3





DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°